I_{DDS}/V_P

A clear understanding of the impact of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that $V_{BE} = 0.7$ V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration. For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}. The number of similarities between the analysis of BJT and JFET dc configurations will become quite apparent in Chapter 6.

5.7 DEPLETION-TYPE MOSFET

As noted in the chapter introduction, there are two types of FETs: JFETs and MOSFETs. MOSFETs are further broken down into *depletion type* and *enhancement type.* The terms *depletion* and *enhancement* define their basic mode of operation, while the label MOSFET stands for *m*etal-*o*xide-*s*emiconductor-*f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of each type of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which happens to have characteristics similar to those of a JFET between cutoff and saturation at I_{DSS} but then has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 5.23. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate.* It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that appearing in Fig. 5.23. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a *dielectric* that sets up opposing (as revealed by

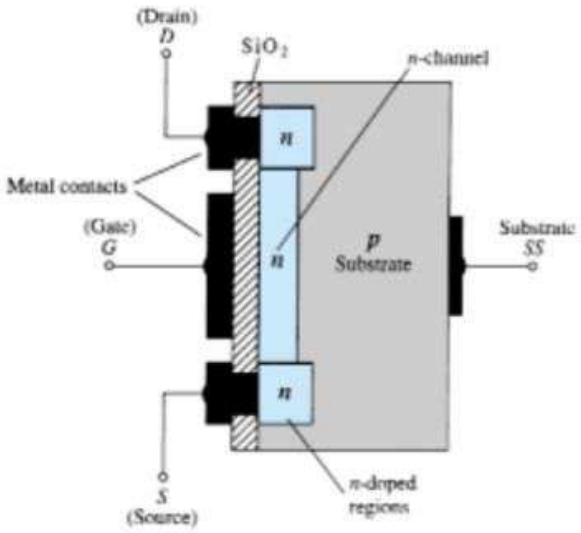

Figure 5.23 *n*-Channel depletion-type MOSFET.

the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer reveals the following fact:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations.

The reason for the label metal-oxide-semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: *insulated-gate FET* or *IGFET,* although this label is used less and less in current literature.

Basic Operation and Characteristics

In Fig. 5.24 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 5.25.

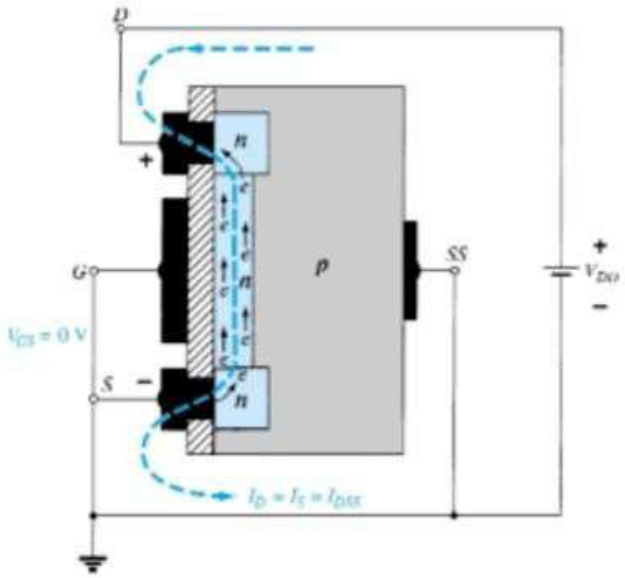

Figure 5.24 *n*-Channel depletion-type MOSFET with $V_{GS} = 0$ V and an applied voltage V_{DD}.

I_{DDS}/V_P

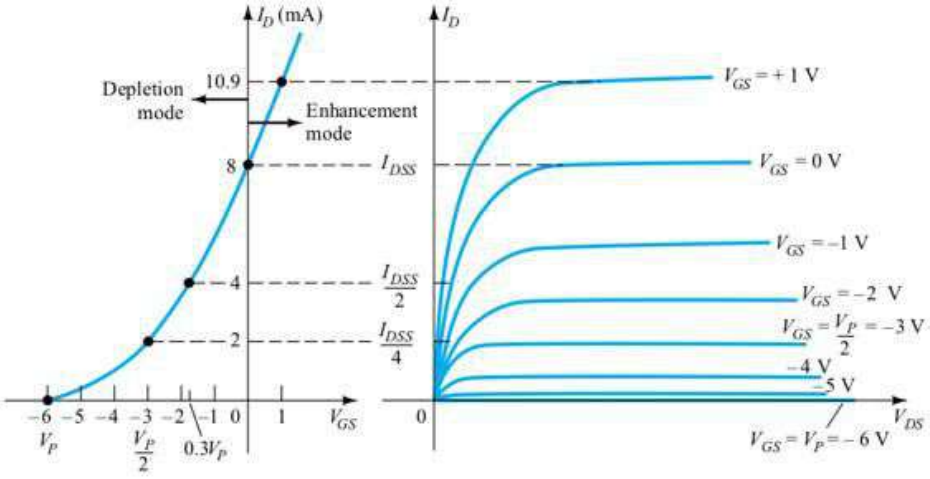

Figure 5.25 Drain and transfer characteristics for an *n*-channel depletion-type MOSFET.

In Fig. 5.26, V_{GS} has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 5.26. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown in Fig. 5.25 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.

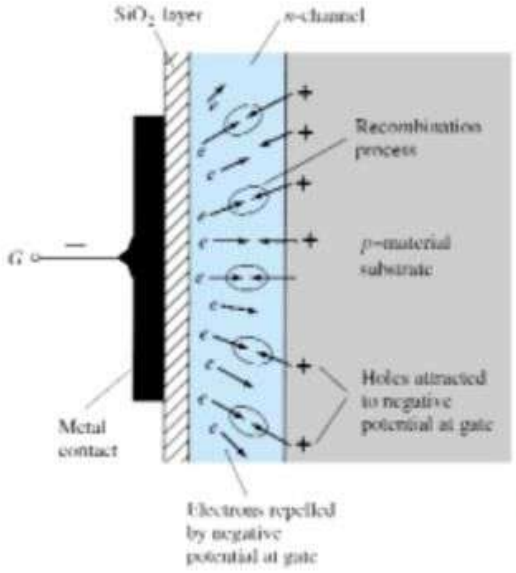

Figure 5.26 Reduction in free carriers in channel due to a negative potential at the gate terminal.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 5.25 reveals that the drain current will increase at a rapid rate for the reasons listed above. The

vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 5.25 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 5.25, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region,* with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region.*

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 5.3

Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution

$$\text{At } V_{GS} = 0 \text{ V}, \qquad I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{GS} = V_P = -4 \text{ V}, \qquad I_D = 0 \text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \qquad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

and at $I_D = \dfrac{I_{DSS}}{2}$, $\qquad V_{GS} = 0.3V_P = 0.3(-4 \text{ V}) = -1.2 \text{ V}$

all of which appear in Fig. 5.27.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we will try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10 \text{ mA}\left(1 - \frac{+1 \text{ V}}{-4 \text{ V}}\right)^2 = 10 \text{ mA}(1 + 0.25)^2 = 10 \text{ mA}(1.5625)$$

$$\cong 15.63 \text{ mA}$$

which is sufficiently high to finish the plot.

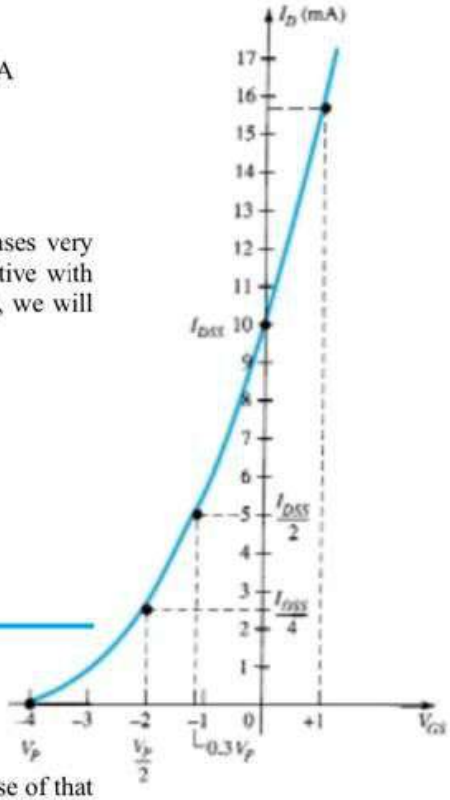

Figure 5.27 Transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 5.23. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 5.28a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 5.25 but with V_{DS} having negative val-